We are in the middle of a digital revolution, resulting from multiple levels of innovation such as the transistor, integrated circuit, microprocessor, and DSP Communications have been revolutionized by digital signal processors. Entertainment is being revolutionized. The question is simple: Is there a third wave of this revolution? Are we at the end of the digital revolution? Examine how we got here, then explore what is to come.

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Keynote Speakers

Gene Frantz, principal fellow for DSP Systems/Texas Instruments We are in the middle of a digital revolution, resulting from multiple levels of innovation such as the transistor, integrated circuit, microprocessor, and DSP Communications have been revolutionized by digital signal processors. Entertainment is being revolutionized. The question is simple: Is there a third wave of this revolution? Are we at the end of the digital revolution? Examine how we got here, then explore what might be the third wave of the digital revolution.

System-Level Implications of Nanometer Design: Commercial EDA Opportunity or Nano-Kiln? 8:30-9:30 a.m. Monday, Oct. 15 Serge Lafl, General Manager, System-Level Engineering Division, Mentor Graphics

It is widely believed nanometer design will become increasingly common. In addition to challenging physical design and verification tools, this trend will force engineers to face and address serious problems in system-level design. Serge Lafl, general manager of the System-Level Engineering Division at Mentor Graphics, leads two business units focused on markets where system-level design plays a pivotal role. Prior to Mentor Graphics, Lafl was responsible for Silicon Graphics' design automation, where his team created revolutionary high-speed simulation tools to enable the design of high-speed 3D graphics chips that defined state-of-the-art in visualization, imaging, and gaming, and special effects for a decade.

Nanosciences: Retrospect and Prospect 8:30-9:30 a.m. Tuesday, Oct. 16

James Meindl, Director of the Joseph M. Pettit Microelectronics Research Center and the Joseph M. Pettit Chair Professor of Microelectronics, Georgia Institute of Technology

The most important economic development of the 20th century was the information revolution. The principal driver of the information revolution is the silicon microchip for two salient reasons. From 1960 to 2006, the productivity of microchip technology increased by more than one billion times and simultaneously, performance increased by more than 100,000 times. Silicon microchip technology is approaching both physical and economic limits that are expected to severely curtail its rate of advance. Intensive exploratory research is aimed at discovering the next technology to propel the information revolution for the first half of the 21st century and beyond.

James Meindl, director of the Joseph M. Pettit Microelectronics Research Center and the Joseph M. Pettit Chair Professor of Microelectronics, is the founding director of the new Nanotechnology Research Center. His research focuses on physical limits on gigascale integration and nanotechnology. A Life Fellow of IEEE and the American Association for the Advancement of Science, Meindl is a member of the American Academy of Arts and Sciences and the National Academy of Engineering.

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Atlanta, GA 30309
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Venue

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Venue

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Keep Pace with Ever-Changing Chip Technology
Exchange Ideas and Share Research at VLSI-SoC 2007 in Atlanta

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**Keep Pace with Ever-Changing Chip Technology**

How do you stay current in a fast-moving, ever-changing field? Chips are using newer technologies and integrating more components on a regular basis. Today’s innovative technology will be obsolete tomorrow. 

Staying one step ahead of innovation requires knowing about latest research and how it affects trends. Chip research responds to consumer demands and offers innovative technologies that help drive that demand.

Join us Monday-Wednesday, Oct. 15-17, as we explore state-of-the-art technology and developments in Very Large Scale Integration Systems and Systems on Chips.

**Why Attend?**

- Make research contacts for future projects
- Discover the latest in chip research and development
- Real ideas to industry feedback
- Pose problems for the academic community
- Get technical solutions to today’s challenges

**Who Should Attend?**

- Logic designers
- Circuit designers
- Analog designers
- Mixed-signal engineers
- Physical designers

**Organized By:**

IFIP Working Group 10.5

**The PIP Working Group 10.5 “Design and Engineering of Electronic Systems” provides a forum for creative experts to explore problem areas and solutions for the design of such complex electronic systems and also disseminates the solutions to a broader industrial and educational sphere. The group belongs to the IFIP Technical Committee 10 and was established in 1994 by merging the old 10.2 and 10.5 working groups.**


**The Council on Electronic Design Automation**


The objectives of IEEE/CEDA include fostering design automation of electronic circuits and systems at all levels through such conferences, workshops and volunteer activities. For more information, visit [http://vlsisoc2007.dlpe.gatech.edu/about.php](http://vlsisoc2007.dlpe.gatech.edu/about.php).

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<td>9:30-10 a.m.</td>
<td>Keynote: Sergei Lev, Vincent Money</td>
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<td>Session 1 Analog Circuit Design</td>
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<tr>
<td>10-11 a.m.</td>
<td>Session 11 Physical Design and Test</td>
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**Session 2 CAD Tools**

Chair: Wayne Wolf (Georgia Tech)

B2.1 “P4CUP: a Parallel and Pipelined Architecture for Regular Expressions”

B2.2 “Use of Gray Encoding for Implementation of Symmetric Functions”

B2.3 “A New Analytical Approach of the Impact of Jitter on Continuous Time Delta Sigma Converters”

B2.4 “A New Analytical Approach of the Performance of a Reconfigurable Hardware-based Architecture for TCP/IP Stack”

**Session 3 Testing and Simulation**

Chair: David Alieno Alonzo (Universidade de Lisboa) in 2004

3.1 “Hierarchical Statistical Analysis of Performance Variation for Continuous-Time Delta-Sigma Modulators”

3.2 “First Order Quasi-Static SOI MOSFET Channel Capacitance Model”

3.3 “Regression Based Beta Models for Accurate Performance Estimation of Analog Circuits”

**Session 5 Communication**

Chair: Vincent Money (Georgia Tech)

5.1 “VLSI Models of Network-on-Chip Interconnect”

5.2 “Statistical Analysis of Systematic and Random Variability of Flip-Flop Race Immunity in 130nm and 90 nm CMOS Technologies”

5.3 “AC Coupling Strategy for High-Speed Transceivers of 10-Gbps and Beyond”

**Session 6 Special Session 1 Reconfigurable and Hybrid Systems**

Chair: Holen-Sean Lee (Georgia Tech)

6.1 “Computing and Design for Softwares and Silicon Manufacturing”

6.2 “Adaptive Genetic Algorithm for Dynamically Reconfigurable Modules Allocation”

6.3 “New Architectures and Adaptive Reconfigurable Computing”

**Session 11 Physical Design and Test**

Chair: Eugene Frantz (Chair)

11.1 “Incremental Placement for Structured ASICs Using the Transportation Driven High-Level Synthesis”

11.2 “Test Data Compression and TAM Design”

11.3 “Dynamic Gates with Hysteretic and Configurable Noise Tolerance”

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**Session 15 New Devices for Mixed Signal**

Chair: Salvador Mir (IMM)

15.1 “A Custom Design of a Three-Stage Amplifier with 500MHz f0 and 1GHz fmax”

15.2 “A 12dBm Dynamic Range 14B Bandwidth Wes ADEC with 114B THD”

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**Posters**

**Session 5 Communication**

Chair: Hsien-Hsin Sean Lee (Georgia Tech)

5.4 “A Permutation Approach for Efficient Timing Closure with a Transistor Level Design Flow”

**Session 9 Special Purpose Design Optimization**

Chair: Qinru Qiu (Binghamton Univ.)

9.1 “Rate-Based Scheduling Policy for Data Flow in Networks on Chip”

9.2 “Parallelizable 3D Scan Multiple Montgomery Multiplier”

9.3 “An Efficient Heterogeneous Reconfigurable Functional Unit for an Adaptive Dynamic External Memory”

**Session 14 Estimation and Evaluation**

Chair: Young Ye (Univ. of Connecticut)


14.2 “Adaptive Genetic Algorithm for Dynamically Reconfigurable Modules Allocation”

14.3 “New Architectures and Adaptive Reconfigurable Computing”

**Session 16 Low Power Design**

Chair: Dieter Kasper (University of Kentucky)

16.1 “A 95mW, Scalable and Unified Montgomery Multiplier Architecture for FPGA and ASIC”

16.2 “Low Power On-Chip Thermal Sensors Based on Wires”

16.3 “Low Power CAM with 10-Transistor Design Cell”

**Demonstration**

“Optimizing DSP Algorithms for Hardware Implementation”

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**VLSI-Soc 2007**

Monday-Wednesday, Oct. 15-17, 2007

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